Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Previously Presented) A registered memory module, comprising:

a register receiving a plurality of input signals at respective input terminals, the register storing the input signals responsive to a transition of an internal clock signal applied to a clock terminal when an enable signal is active, the register having output terminals to which the stored input signals are coupled;

a plurality of memory devices coupled to the output terminals of the register; and

a logic circuit applying the enable signal to the register, the logic circuit being structured to make the enable signal active responsive to one of the memory devices in the memory module being accessed.

Claims 2-45 (Canceled)

46. (Previously Presented) The registered memory module of claim 1 wherein the logic circuit is further structured to make the enable signal inactive when one of the memory devices in the memory module is not being accessed.

47. (Previously Presented) The registered memory module of claim 1 wherein the register comprises a plurality of flip-flops each having a data terminal receiving a respective one of the input signals and a clock terminal receiving the clock signal.

48. (Previously Presented) The registered memory module of claim 47 wherein each of the flip-flops includes an enable terminal coupled to receive the enable signal

from the logic circuit, the flip-flops latching the input signals applied to respective data terminals responsive to the enable signal being active.

49. (Previously Presented) The registered memory module of claim 48 wherein the logic circuit comprises a NAND gate.

50. (Previously Presented) The registered memory module of claim 1 wherein the register comprises:

a plurality of logic gates each having a first input terminal to which a respective one of the input signals is coupled and a second input terminal to which the enable signal is coupled, each of the logic gates having an output terminal; and

a plurality of flip-flops each having a data terminal coupled to the output terminal of a respective one of the logic gates and a clock terminal receiving the clock signal.

51. (Previously Presented) The registered memory module of claim 1 wherein each of the memory devices comprise a dynamic random access memory ("DRAM") device.

52. (Previously Presented) The registered memory module of claim 51 wherein each of the DRAM devices comprise a synchronous DRAM device.

53. (Previously Presented) The registered memory module of claim 1 wherein the memory module further receives a clock enable signal, and wherein the clock enable signal is stored in the register.

54. (Previously Presented) The registered memory module of claim 1 wherein the input signals comprise address signals.

55. (Previously Presented) A memory module, comprising:

a receiver circuit receiving a plurality of signals at respective input terminals, the receiver circuit inputting the signals responsive to a transition of an internal clock signal applied to a clock terminal when an enable signal is active, the receiver circuit having output terminals to which the input signals are coupled when the enable signal is active;

a plurality of memory devices coupled to the output terminals of the receiver circuit, each of the memory devices being selected by a respective select signal being active; and

a logic circuit receiving the select signals for the memory devices and applying the enable signal to the receiver circuit, the logic circuit being structured to make the enable signal active responsive to any of the select signals being active and to make the enable signal inactive response to none of the select signals being active.

56. (Previously Presented) The memory module of claim 55 wherein the receiver circuit comprises a plurality of flip-flops each having a data terminal receiving a respective one of the input signals and a clock terminal receiving the clock signal.

57. (Previously Presented) The memory module of claim 56 wherein each of the flip-flops includes an enable terminal coupled to receive the enable signal from the logic circuit, the flip-flops latching the input signals applied to respective data terminals responsive to the enable signal being active.

58. (Previously Presented) The memory module of claim 57 wherein the logic circuit comprises a NAND gate.

59. (Previously Presented) The memory module of claim 55 wherein the receiver circuit comprises:

a plurality of logic gates each having a first input terminal to which a respective one of the input signals is coupled and a second input terminal to which the enable signal is coupled, each of the logic gates having an output terminal; and

a plurality of flip-flops each having a data terminal coupled to the output terminal of a respective one of the logic gates and a clock terminal receiving the clock signal.

60. (Previously Presented) The memory module of claim 59 wherein the logic circuit comprises an AND gate.

61. (Previously Presented) The memory module of claim 55 wherein each of the memory devices comprise a dynamic random access memory ("DRAM") device.

62. (Previously Presented) The memory module of claim 61 wherein each of the DRAM devices comprise a synchronous DRAM device.

63. (Previously Presented) The memory module of claim 55 wherein the memory module further receives a clock enable signal, and wherein the clock enable signal is coupled to the output terminals of the receiver circuit.

64. (Previously Presented) The memory module of claim 55 wherein the input signals comprise address signals.

65. (Previously Presented) The memory module of claim 55 wherein the input signals further comprise the select signals.

66. (Previously Presented) The memory module of claim 56 wherein the receiver circuit comprises a register that is operable to store the input signals.

67. (Previously Presented) A memory module, comprising:

a receiver circuit receiving a plurality of signals at respective input terminals, the receiver circuit inputting the signals responsive to a transition of an internal clock signal applied

to a clock terminal when an enable signal is active, the receiver circuit having output terminals to which the input signals are coupled when the enable signal is active;

a plurality of memory devices coupled to the output terminals of the receiver circuit; and

a logic circuit applying the enable signal to the receiver circuit, the logic circuit being structured to make the enable signal active responsive to one of the memory devices in the memory module being accessed.

68. (Previously Presented) The memory module of claim 67 wherein the logic circuit is further structured to make the enable signal inactive when one of the memory devices in the memory module is not being accessed.

69. (Previously Presented) The memory module of claim 67 wherein the receiver circuit comprises a plurality of flip-flops each having a data terminal receiving a respective one of the input signals and a clock terminal receiving the clock signal.

70. (Previously Presented) The memory module of claim 69 wherein each of the flip-flops includes an enable terminal coupled to receive the enable signal from the logic circuit, the flip-flops latching the input signals applied to respective data terminals responsive to the enable signal being active.

71. (Previously Presented) The memory module of claim 67 wherein the receiver circuit comprises:

a plurality of logic gates each having a first input terminal to which a respective one of the input signals is coupled and a second input terminal to which the enable signal is coupled, each of the logic gates having an output terminal; and

a plurality of flip-flops each having a data terminal coupled to the output terminal of a respective one of the logic gates and a clock terminal receiving the clock signal.

72. (Previously Presented) The memory module of claim 67 wherein each of the memory devices comprise a dynamic random access memory ("DRAM") device.

73. (Previously Presented) The memory module of claim 72 wherein each of the DRAM devices comprise a synchronous DRAM device.

74. (Previously Presented) The memory module of claim 67 wherein the memory module further receives a clock enable signal, and wherein the clock enable signal is coupled to the output terminals of the receiver circuit.

75. (Previously Presented) The memory module of claim 67 wherein the input signals comprise address signals.

76. (Previously Presented) The memory module of claim 67 wherein the receiver circuit comprises a register that is operable to store the input signals.

77. (Previously Presented) A computer system, comprising:

a central processing unit ("CPU");

a system controller coupled to the CPU;

an input device coupled to the CPU through the system controller;

an output device coupled to the CPU through the system controller;

a storage device coupled to the CPU through the system controller; and

at least one registered memory module coupled to the CPU through the system controller, the at least one registered memory module comprising:

a register receiving a plurality of input signals at respective input terminals, the register storing the input signals responsive to a transition of an internal clock signal applied to a clock terminal when an enable signal is active, the register having output terminals to which the stored input signals are coupled;

a plurality of memory devices coupled to the output terminals of the register; and

a logic circuit applying the enable signal to the register, the logic circuit being structured to make the enable signal active responsive to one of the memory devices in the memory module being accessed.

78. (Previously Presented) The computer system of claim 77 wherein the logic circuit is further structured to make the enable signal inactive when one of the memory devices in the memory module is not being accessed.

79. (Previously Presented) The computer system of claim 77 wherein the register comprises a plurality of flip-flops each having a data terminal receiving a respective one of the input signals and a clock terminal receiving the clock signal.

80. (Previously Presented) The computer system of claim 79 wherein each of the flip-flops includes an enable terminal coupled to receive the enable signal from the logic circuit, the flip-flops latching the input signals applied to respective data terminals responsive to the enable signal being active.

81. (Previously Presented) The computer system of claim 80 wherein the logic circuit comprises a NAND gate.

82. (Previously Presented) The computer system of claim 77 wherein the register comprises:

a plurality of logic gates each having a first input terminal to which a respective one of the input signals is coupled and a second input terminal to which the enable signal is coupled, each of the logic gates having an output terminal; and

a plurality of flip-flops each having a data terminal coupled to the output terminal of a respective one of the logic gates and a clock terminal receiving the clock signal.

83. (Previously Presented) The computer system of claim 77 wherein each of the memory devices comprise a dynamic random access memory ("DRAM") device.

84. (Previously Presented) The computer system of claim 83 wherein each of the DRAM devices comprise a synchronous DRAM device.

85. (Previously Presented) The computer system of claim 77 wherein the memory module further receives a clock enable signal, and wherein the clock enable signal is stored in the register.

86. (Previously Presented) The computer system of claim 77 wherein the input signals comprise address signals.

87. (Previously Presented) A computer system, comprising:

a central processing unit ("CPU");

a system controller coupled to the CPU;

an input device coupled to the CPU through the system controller;

an output device coupled to the CPU through the system controller;

a storage device coupled to the CPU through the system controller; and

at least one memory module coupled to the CPU through the system controller, the at least one memory module comprising:

a receiver receiving a plurality of input signals at respective input terminals, the receiver coupling the input signals to respective output terminals responsive to a transition of an internal clock signal applied to a clock terminal when an enable signal is active;

a plurality of memory devices coupled to the output terminals of the receiver, each of the memory devices being selected by a respective select signal being active; and

a logic circuit receiving the select signals for the memory devices and applying the enable signal to the register, the logic circuit being structured to make the enable signal active responsive to any of the select signals being active and to make the enable signal inactive response to none of the select signals being active.

88. (Previously Presented) The computer system of claim 87 wherein the receiver comprises a plurality of flip-flops each having a data terminal receiving a respective one of the input signals and a clock terminal receiving the clock signal.

89. (Previously Presented) The computer system of claim 88 wherein each of the flip-flops includes an enable terminal coupled to receive the enable signal from the logic circuit, the flip-flops latching the input signals applied to respective data terminals responsive to the enable signal being active.

90. (Previously Presented) The computer system of claim 89 wherein the logic circuit comprises a NAND gate.

91. (Previously Presented) The computer system of claim 87 wherein the receiver comprises:

a plurality of logic gates each having a first input terminal to which a respective one of the input signals is coupled and a second input terminal to which the enable signal is coupled, each of the logic gates having an output terminal; and

a plurality of flip-flops each having a data terminal coupled to the output terminal of a respective one of the logic gates and a clock terminal receiving the clock signal.

92. (Previously Presented) The computer system of claim 87 wherein each of the memory devices comprise a dynamic random access memory ("DRAM") device.

93. (Previously Presented) The computer system of claim 92 wherein each of the DRAM devices comprise a synchronous DRAM device.

94. (Previously Presented) The computer system of claim 87 wherein the input signals comprise address signals.

95. (Previously Presented) The computer system of claim 87 wherein the input signals further comprise the select signals.

96. (Previously Presented) A method of accessing a plurality of memory devices coupled to a receiver that receives a plurality of input signals, the method comprising:

determining whether or not a memory access is directed to any of the memory devices;

periodically coupling the input signals to respective output terminals of the receiver responsive to determining that the memory access is directed to any of the memory devices; and

refraining from periodically coupling the input signals to respective output terminals of the receiver responsive to determining that the memory access is not directed to any of the memory devices; and

coupling the input signals from the output terminals to at least one of the memory devices.

97. (Previously Presented) The method of claim 96 wherein respective select signals are applied to each of the memory devices to enable their operation, and wherein the act of determining whether or not a memory access is directed to any of the memory devices comprises examining the select signals and determining if any of the select signals have a predetermined state.

98. (Previously Presented) The method of claim 96 wherein the acts of periodically coupling the input signals to respective output terminals and refraining from periodically coupling the input signals to respective output terminals comprise:

coupling the input signals to the receiver through respective logic gates;

enabling the logic gates responsive to determining that the memory access is directed to any of the memory devices; and

disabling the logic gates responsive to determining that the memory access is not directed to any of the memory devices.

99. (Previously Presented) The method of claim 96 wherein the receiver is operable to couple the input signals to respective output terminals responsive to a clock signal when the receiver is enabled by an enable signal, and wherein the acts of periodically coupling the input signals to respective output terminals and refraining from periodically coupling the input signals to respective output terminals comprise:

coupling the input signals to the receiver;

enabling the receiver responsive to determining that the memory access is directed to any of the memory devices; and

disabling the receiver responsive to determining that the memory access is not directed to any of the memory devices.

100. (Previously Presented) The method of claim 96 wherein the act of periodically coupling the input signals to respective output terminals comprises periodically coupling the address signals to respective output terminals .

101. (Previously Presented) The method of claim 96 wherein each of the memory devices comprises a dynamic random access memory ("DRAM") device.

102. (Previously Presented) The method of claim 101 wherein each of the DRAM devices comprises a synchronous DRAM device.

103. (Previously Presented) The method of claim 96 wherein the act of periodically coupling the input signals to respective output terminals comprises periodically coupling to respective output terminals respective select signals selecting the memory devices for memory accesses.

104. (Previously Presented) In a memory module having an input circuit for performing an operation on input signals responsive to a clock signal and coupling signals resulting from the input signals to a plurality of memory devices in the module, a method of reducing the power consumed by the memory module, comprising:

determining whether or not a memory access is directed to any of the memory devices in the module;

enabling the input circuit to perform the operation on the input signals responsive to determining that the memory access is directed to any of the memory devices; and

disabling the input circuit from perform the operation on the input signals responsive to determining that the memory access is not directed to any of the memory devices.

105. (Previously Presented) The method of claim 104 wherein respective select signals are applied to each of the memory devices to enable their operation, and wherein the act of determining whether or not a memory access is directed to any of the memory devices comprises examining the select signals and determining if any of the select signals have a predetermined state.

106. (Previously Presented) The method of claim 104 wherein the input signals comprise address signals.

107. (Previously Presented) The method of claim 104 wherein each of the memory devices comprises a dynamic random access memory ("DRAM") device.

108. (Previously Presented) The method of claim 107 wherein each of the DRAM devices comprises a synchronous DRAM device.